

CLAIMS

1. A method for transitioning a debugging unit between a plurality of operating states, comprising:
defining a first set of operating instructions to be processed by a processor core;
defining a first triggering instruction to provide a first signal to the debugging unit whereby the debugging unit is operable to transition from a first operating state to a second operating state; and
embedding said first triggering instruction within said first set of operating instructions.
2. The method of claim 1, further comprising:
coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction;
operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a second signal representative of said coded first triggering instruction; and
operating said processor core to provide said first signal to the debugging unit in response to said second signal to thereby transition the debugging unit from the first operating state to the second operating state.

3. The method of claim 1, further comprising:

defining a second triggering instruction to provide a second signal to the debugging unit whereby the debugging unit is operable to transition from the second operating state to the first operating state; and

embedding said second triggering instruction within said first set of operating instructions.

4. The method of claim 3, further comprising:

coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction and a coded second triggering instruction;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a third signal representative of said coded first triggering instruction and a fourth signal representative of said coded second triggering instruction;

operating said processor core to provide said first signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first operating state to the second operating state; and

subsequent to providing said first signal to the debugging unit, operating said processor core to provide said second signal to the debugging unit in response to said fourth signal to thereby transition the debugging unit from the second operating state to the first operating state.

5. The method of claim 1, further comprising:

defining a second triggering instruction to provide a second signal to the debugging unit whereby the debugging unit is operable to transition from the second operating state to a third operating state; and

embedding said second triggering instruction within said first set of operating instructions.

6. The method of claim 5, further comprising:

coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction and a coded second triggering instruction;

operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a third signal representative of said coded first triggering instruction and a fourth signal representative of said coded second triggering instruction;

operating said processor core to provide said first signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first operating state to the second operating state; and

subsequent to providing said first signal to the debugging unit, operating said processor core to provide said second signal to the debugging unit in response to said fourth signal to thereby transition the debugging unit from the second operating state to the third operating state.

7. The method of claim 1, further comprising:
defining a second set of operating instructions to
generate a first data or a second data; and
embedding said second set of operating instructions
5 within said first set of operating instructions.

8. The method of claim 7, further comprising:
coding said first set of operating instructions within
a computer readable medium, said first set of operating
10 instructions including a coded first triggering instruction and a
coded second set of operating instructions;

operating said computer readable medium to provide an
instruction stream to a processor core, said instruction stream
representative of said coded first set of operating instructions,
15 said instruction stream including a second signal representative
of said coded first triggering instruction and a set of signals
representative of said coded second set of operating
instructions;

operating said processor core to generate said first
20 data or said second data in response to said set of signals; and

subsequent to a generation of said first data by said
processor core, operating said processor core to provide said
first signal to the debugging unit in response to said second
signal to thereby transition the debugging unit from the first
25 operating state to the second operating state.

9. The method of claim 1, further comprising:
further defining said first triggering instruction to
provide a second signal to the debugging unit whereby the
debugging unit is operable to transition from the first operating
5 state to a third operating state;
defining a second set of operating instructions to
generate either a first data or a second data; and
embedding said second set of operating instructions
within said first set of operating instructions.

10. The method of claim 9, further comprising:
coding said first set of operating instructions within
a computer readable medium, said first set of operating
instructions including a coded first triggering instruction, and
15 a coded second set of operating instructions;
operating said computer readable medium to provide an
instruction stream to a processor core, said instruction stream
representative of said coded first set of operating instructions,
said instruction stream including a third signal representative
20 of said coded first triggering instruction, and a set of signals
representative of said coded second set of operating
instructions;
operating said processor core to generate either said
first data or said second data in response to said set of
25 signals;
subsequent to a generation of said first data by said
processor core, operating said processor core to provide said
first signal to the debugging unit in response to said third
signal to thereby transition the debugging unit from the first
30 operating state to the second operating state; and
subsequent to a generation of said second data by said
processor core, operating said processor core to provide said
second signal to the debugging unit in response to said third
signal to thereby transition the debugging unit from the first
35 operating state to the third operating state.

11. A microprocessor, comprising:

a debugging unit operable to transition from a first operating state to a second operating state in response to a first signal; and

a processor core operable to fetch an instruction stream including a second signal representative of a first triggering instruction to transition said debugging unit from said first operating state to said second operating state, said processor core further operable to provide said first signal to said debugging unit in response to said second signal.

12. The microprocessor of claim 11,

wherein said processor core includes a register operable to provide said first signal to said debugging unit in response to a third signal including an address of said register.

13. The microprocessor of claim 11, wherein

said debugging unit is further operable to transition from said second operating state to said first operating state in response to a third signal;

said instruction stream further includes a fourth signal representative of a second triggering instruction to transition said debugging unit from said second operating state to said first operating state; and

said processor core is further operable to provide said third signal to said debugging unit in response to said fourth signal.

14. The microprocessor of claim 13,
wherein said processor core includes
a first register operable to provide said first signal
to said debugging unit in response to a fifth signal including an
5 address of said first register; and
a second register operable to provide said third signal
to said debugging unit in response to a sixth signal including an
address of said second register.

10 15. The microprocessor of claim 11, wherein
said debugging unit is further operable to transition
from said second operating state to a third operating state in
response to a third signal;
said instruction stream further includes a fourth
15 signal representative of a second triggering instruction to
transition said debugging unit from said second operating state
to said third operating state; and
said processor core is further operable to provide said
20 third signal to said debugging unit in response to said fourth
signal.

25 16. The microprocessor of claim 15,
wherein said processor core includes
a first register operable to provide said first signal
to said debugging unit in response to a fifth signal including an
address of said first register; and
a second register operable to provide said third signal
to said debugging unit in response to a sixth signal including an
address of said second register.

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17. The microprocessor of claim 11, wherein
said instruction stream further includes a set of
signals representative of a set of operating instructions to
operate said processor core to generate a first data or a second
data;

said processor core is further operable to generate said first data or said second data in response to said set of signals; and

subsequent to a generation of said trigger data, said processor core is further operable to provide said first signal to said debugging unit in response to said second signal.

18. The microprocessor of claim 17,
wherein said processor core includes a register
operable to provide said second signal to said debugging unit in
response to a third signal including an address of said register
and a fourth signal including said first data.

19. The microprocessor of claim 11, wherein
said debugging unit is further operable to transition
from said first operating state to a third operating state in
response to a third signal;

5 said first trigger instruction is to selectively
transition said debugging unit from said first operating state to
said second operating state or to transition said debugging unit
from said first operating state to said third operating state;

10 said instruction stream further includes a set of
signals representative of a set of operating instructions to
operate said processor core to generate a first data or a second
data;

15 said processor core is further operable to selectively
generate said first trigger data or said second trigger data in
response to said set of signals;

20 subsequent to a generation of said first data, said
processor core is further operable to provide said first signal
to said debugging unit in response to said second signal; and

25 subsequent to a generation of said second data, said
processor core is operable to provide said third signal to said
debugging unit in response to said second signal.

20. The microprocessor of claim 19,

25 wherein said processor core includes a register
operable to provide said first signal to said debugging unit in
response to a fourth signal including an address of said register
and a fifth signal including said first data, and operable to
provide said third signal to said debugging unit in response to a
30 sixth signal including an address of said register and a seventh
signal including said second data.

21. A computer readable medium storing a program for transitioning a debugging unit between a plurality of operating states, comprising:

a first computer readable code to operate a processor core; and

a second computer readable code to transition the debugging unit from a first operating state to a second operating state, said second computer readable code embedded within said first computer readable code.

22. The computer readable medium of claim 21, further comprising:

a third computer readable code to transition the debugging unit from said second operating state to said first operating state, said third computer readable code embedded within said first computer readable code.

23. The computer readable medium of claim 21, further comprising:

a third computer readable code to transition the debugging unit from said second operating state to a third operating state, said third computer readable code embedded within said first computer readable code.

24. The computer readable medium of claim 21, further comprising:

a third computer readable code to operate said processor core to generate a first data or a second data, said third computer readable code embedded within said first computer readable code,

wherein said second computer readable code is to transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data.

25. The computer readable medium of claim 21, further comprising:

a third computer readable code to operate said processor core to generate a first data or a second data, said
5 third computer readable code embedded within said first computer readable code,

wherein said second computer readable code is to transition the debugging unit from said first operating state to said second operating state in response to a generation of said
10 first data, and wherein said second computer readable code is to transition the debugging unit from said first operating state to a third operating state in response to a generation of said second data.

26. A system for transitioning a debugging unit between a plurality of operating states, comprising:

a computer readable medium including a first computer readable code to transition the debugging unit from a first operating state to a second operating state, said computer
20 readable medium operable to provide a first signal representative of said first computer readable code; and

a processor core operable to provide a second signal to the debugging unit in response to said first signal whereby the debugging unit is operable to transition from the first operating
25 state to the second operating state.

27. The system of claim 26,

wherein said processor core includes a register operable to provide said second signal in response to a third
30 signal including an address of said register.

28. The system of claim 27, wherein
said computer readable medium further includes a second
computer readable code to transition the debugging unit from the
second operating state to the first operating state, said
5 computer readable medium operable to provide a third signal
representative of said second computer readable code; and
said processor core is further operable to provide a
fourth signal to the debugging unit in response to said third
signal whereby the debugging unit is operable to transition from
10 the second operating state to the first operating state.

29. The system of claim 28,
wherein said processor core includes
a first register operable to provide said second signal
15 to the debugging unit in response to a fifth signal including an
address of said first register; and
a second register operable to provide said fourth
signal to the debugging unit in response to a sixth signal
including an address of said second register.

30. The system of claim 27, wherein
said computer readable medium further includes a second
computer readable code to transition the debugging unit from the
second operating state to a third operating state, said computer
25 readable medium operable to provide a third signal representative
of said second computer readable code; and
said processor core is further operable to provide a
fourth signal to the debugging unit in response to said third
signal whereby the debugging unit is operable to transition from
30 the second operating state to the third operating state.

31. The system of claim 30, wherein
said processor core includes

a first register operable to provide said second signal to the debugging unit in response to a fifth signal including an address of said first register; and

5 a second register operable to provide said fourth signal to the debugging unit in response to a sixth signal including an address of said second register.

32. The system of claim 27, wherein

10 said computer readable medium further includes a second computer readable code to operate said processor core to generate a first trigger data or a second trigger data, said computer readable medium operable to provide a set of signals representative of said second computer readable code;

15 said processor core is further operable to selectively generate said trigger data in response to said set of signals; and

20 subsequent to a generation of said first data, said processor core is operable to provide said first signal to the debugging unit in response to said second signal.

33. The system of claim 32,

25 wherein said processor core includes a register operable to provide said second signal to the debugging unit in response to a third signal including an address of said register and a fourth signal including said trigger data.

34. The system of claim 27, wherein

said first computer readable code is to selectively transition the debugging unit from the first operating state to the second operating state or from the first operating state to a third operating state;

said computer readable medium further includes a second computer readable code to operate said processor core to generate a first data or a second data, said computer readable medium operable to provide a set of signals representative of said second computer readable code;

said processor core is further operable to selectively generate said first data or said trigger data in response to said set of signals;

subsequent to a generation of said first data, said processor core is operable to provide said second signal to the debugging unit in response to said first signal; and

subsequent to a generation of said second data, said processor core is operable to provide a fourth signal to the debugging unit in response to said first signal whereby the debugging unit is operable to transition from the first operating state to the third operating state.

35. The system of claim 34,

wherein said processor core includes a register operable to provide said second signal to the debugging unit in response to a fourth signal including an address of said register and a fifth signal including said first data, and to provide said third signal to the debugging unit in response to a sixth signal including said address of said register and a seventh signal including said second data.

36. A method for transitioning a debugging unit between a plurality of operating states, comprising:

receiving a first signal representative of a first triggering instruction to transition the debugging unit from a first operating state to a second operating state; and

processing said first signal to thereby transition the debugging unit from said first operating state to said second operating state.

37. The method of claim 36,

receiving a second signal representative of a second triggering instruction to transition the debugging unit from said second operating state to said first operating state; and

processing said second signal to thereby transition the debugging unit from said second operating state to said first operating state.

38. The method of claim 36,

receiving a second signal representative of a second triggering instruction to transition the debugging unit from said second operating state to a third operating state; and

processing said second signal to thereby transition the debugging unit from said second operating state to said third operating state.

39. A method for transitioning a debugging unit between a plurality of operating states, comprising:

receiving a set of operating signals representative of a set of operating instructions to generate a first data or a second data;

receiving a trigger instruction signal representative of a triggering instruction to transition the debugging unit from a first operating state to a second operating state in response to a generation of said first data; and

processing said set of operating signals and said trigger instruction signal to thereby transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data.

40. A method for transitioning a debugging unit between a plurality of operating states, comprising:

receiving a set of operating signals representative of a set of operating instructions to generate a first data or a second data;

receiving a trigger instruction signal representative of a triggering instruction to transition the debugging unit from a first operating state to a second operating state in response to a generation of said first data and to transition the debugging unit from said first operating state to a third operating state in response to a generation of said second data; and

processing said set of operating signals and said trigger instruction signal to thereby transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data and to thereby transition the debugging unit from said first operating state to said third operating state in response to a generation of said second data.

41. A method, comprising:

providing a computer readable medium operable to provide a first signal representative of a first triggering instruction to transition a debugging unit from a first operating state to a second operating state;

providing a processor core operable to provide a second signal in response to said first signal; and

providing a debugging unit operable to transition from said first operating state to said second operating state in response to said second signal.

42. A method, comprising:

providing a computer readable medium operable to provide a set of operating signals representative of a set of operating instructions to generate a first data or a second data, and a trigger instruction signal representative of a triggering instruction to transition a debugging unit from a first operating state to a second operating;

providing a processor core operable to generate said first data or said second data in response to said set of operating signals, and to provide a triggering signal subsequent to a generation of said first data in response to said trigger instruction signal; and

providing a debugging unit operable to transition from said first operating state to said second operating state in response to said triggering signal.

43. A method, comprising:

providing a computer readable medium operable to provide a set of operating signals representative of a set of operating instructions to generate a first data or a second data, and a trigger instruction signal representative of a triggering instruction to transition said debugging unit from a first operating state to a second operating state or to transition said debugging unit from said first operating state to a third operating state;

providing a processor core operable to generate said first data or said trigger data in response to said set of operating signal, to provide a first triggering signal subsequent to a generation of said first data in response to said triggering instruction signal, and to provide a second triggering signal subsequent to a generation of said second data in response to said triggering instruction signal; and

providing a debugging unit operable to transition from said first operating state to said second operating state in response to said first triggering signal and to transition from said first operating state to said third operating state in response to said second triggering signal.

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